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10/619,463	07/16/2003	Tetsuya Fukuoka	HITA.0408	7713

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EXAMINER	
IWASHKO, LEV	
ART UNIT	**PAPER NUMBER**
2186	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/619,463	FUKUOKA ET AL.	
	Examiner	Art Unit	
	Lev I. Iwashko	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *16 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *16 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/16/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Miyaoka et al. (US Patent 5,291,445).

Claim 1. A semiconductor integrated circuit provided with an address conversion memory circuit for converting a logical address into a physical address, comprising: *(Column 31, lines 46-49 – State that there is an address translation buffer that converts the logical address into a physical address)*

- a switching circuit which switches to the active or non-active state *(Column 34, lines 37-47 – State that there is a switching circuit that selectively makes connections)*
- a circuit portion including at least a tag memory for storing a logical page address as the upper bits of the logical address and *(Column 31, lines 49-55 – State the following: "The tag memory BAA performs read operations on a plurality of units by association using predetermined bits of the logical addresses as the search data. In case of a "hit," the corresponding tag i.e., the physical address of the data stored in the buffer storage BSA or BSB, is input to the other input terminal of the comparator COM)*
- a data memory for storing a physical page address as the upper bits of the physical address of said address conversion memory circuit, *(Column 31, lines 65-68 and Column 1, lines 1-12 – State the*

following: "In the meantime, read operations on the buffer storages BSA and BSB continue by use of predetermined bits in the logical addresses, in parallel with the compare operation. Stored data is read from the corresponding addresses in a plurality of units, the data being subjected to sequence control provided by the corresponding aligners ALA-ALD. The output signals of these aligners undergo row selection provided by the row selector circuit ROW and are then placed onto the internal bus of the CPU via an output buffer register OBR. Needless to say, if there is no "hit" between the physical address from the address translation buffer TLB and the physical address from the tag memory BAA, the CPU ignores the data read from the units in the buffer storages BSA and BSB, and proceeds with its access to the main storage)

- wherein said circuit portion is set to non-active state with said switching circuit during the period in which the circuit for memory access is in the active state and the circuit portion of said address conversion memory circuit is not used. *(Column 34, lines 12-55 – Describe how the switching circuit selects between the circuit for memory access and address conversion)*

Claim 2. A semiconductor integrated circuit according to claim 1, comprising:

- a setting register which sets an access mode to a main memory to any one of the virtual memory access mode for making access to a virtual memory area with the address conversion of said address conversion memory circuit and the physical memory access mode for making no access to the virtual memory area, *(Column 30, lines 52-55 – State the following: "The CPU of this embodiment operates on, but is not limited by, the virtual storage scheme whereby the address space of the main storage is processed and managed in terms of logical addresses")*

- wherein said switching circuit sets said circuit portion to non-active state based on a state that said access mode is set to said physical memory access mode. *(Column 34, lines 37-47 – State that there is a switching circuit that selectively makes connections)*

Claim 3. A semiconductor integrated circuit according to claim 2, comprising:

- a cache memory which stores data between a processor and the main memory, *(Column 36, lines 7-14 – Mention buffer storage (a.k.a. cache memory))*
- wherein said switching circuit sets said circuit portion to non-active state while the data transfer is performed between said cache memory and main memory *(Column 34, lines 37-47 – State that there is a switching circuit that selectively makes connections)*
- because miss-hit is judged in said cache memory by the memory access of said processor. *(Column 31, lines 56-64 – State the following: "The comparator COM compares the physical address from the address translation buffer TLB with the physical address that is output as the tag from the "hit" unit of the tag memory BAA. In case of a match between these addresses, the comparator COM supplies the row selector circuit ROW with a row selection signal for designating the "hit" unit. At this point, the CPU recognizes the hit in the buffer storage and halts its access to the main storage accordingly")*

Claim 4. A semiconductor integrated circuit according to claim 1, comprising:

- a register for holding the logical page address previously inputted to said address conversion memory circuit; *(Column 10, lines 31-37 – State the following: "This arrangement allows a desired logic gate circuit, and hence a desired logic circuit, to be constructed. As a result, the gate array section GA is illustratively used to construct registers, selector circuits and various arithmetic circuits, the registers holding input and output data of the RAM macrocells")*

- a first comparator for comparing a logical page address of the logical address outputted from the memory access circuit with a value of said register; and *(Column 31, lines 56-64 – State the following: "The comparator COM compares the physical address from the address translation buffer TLB with the physical address that is output as the tag from the "hit" unit of the tag memory BAA. In case of a match between these addresses, the comparator COM supplies the row selector circuit ROW with a row selection signal for designating the "hit" unit. At this point, the CPU recognizes the hit in the buffer storage and halts its access to the main storage accordingly")*
- a second comparator for comparing and judging whether the intra-page address as the remaining lower bits of the relevant logical address is included or not within a boundary area of the address range indicated by the logical page address, *(Column 34, lines 12-21 – Claim ECL differential circuits which act as the proposed second comparator)*
- wherein said switching circuit sets said circuit portion to non-active state when the logical page address is proved to be identical to the preceding logical address based on the result of comparison by said first and second comparators and the intra-page address is not included within said boundary area. *(Column 31, lines 65-68 and Column 32, lines 1-12 – State the following: "In the meantime, read operations on the buffer storages BSA and BSB continue by use of predetermined bits in the logical addresses, in parallel with the compare operation. Stored data is read from the corresponding addresses in a plurality of units, the data being subjected to sequence control provided by the corresponding aligners ALA-ALD. The output signals of these aligners undergo row selection provided by the row selector circuit ROW and are then placed onto the internal bus of the CPU via an output buffer register OBR. Needless to say, if there is no "hit" between the physical address from the address translation buffer TLB*

and the physical address from the tag memory BAA, the CPU ignores the data read from the units in the buffer storages BSA and BSB, and proceeds with its access to the main storage")

Claim 5. A semiconductor integrated circuit according to claim 2, comprising:

- a register for holding the logical page address previously inputted to said address conversion memory circuit; a first comparator for comparing a logical page address of the logical address outputted from the memory access circuit with a value of said register; and *(Column 10, lines 31-37 – State the following: "This arrangement allows a desired logic gate circuit, and hence a desired logic circuit, to be constructed. As a result, the gate array section GA is illustratively used to construct registers, selector circuits and various arithmetic circuits, the registers holding input and output data of the RAM macrocells")*
- a first comparator for comparing a logical page address of the logical address outputted from the memory access circuit with a value of said register; and *(Column 31, lines 56-64 – State the following: "The comparator COM compares the physical address from the address translation buffer TLB with the physical address that is output as the tag from the "hit" unit of the tag memory BAA. In case of a match between these addresses, the comparator COM supplies the row selector circuit ROW with a row selection signal for designating the "hit" unit. At this point, the CPU recognizes the hit in the buffer storage and halts its access to the main storage accordingly")*
- a second comparator for comparing and judging whether the intra-page address as the remaining lower bits of the relevant logical address is included or not within the boundary area of the address range indicated by the logical page address, *(Column 34, lines 12-21 – Claim ECL differential circuits which act as the proposed second comparator)*

- wherein said switching circuit sets said circuit portion to non-active state when the logical page address is proved to be identical to the preceding logical address based on the result of comparison by said first and second comparators and the intra-page address is not included within said boundary area. *(Column 31, lines 65-68 and Column 32, lines 1-12 – State the following: "In the meantime, read operations on the buffer storages BSA and BSB continue by use of predetermined bits in the logical addresses, in parallel with the compare operation. Stored data is read from the corresponding addresses in a plurality of units, the data being subjected to sequence control provided by the corresponding aligners ALA-ALD. The output signals of these aligners undergo row selection provided by the row selector circuit ROW and are then placed onto the internal bus of the CPU via an output buffer register OBR. Needless to say, if there is no "hit" between the physical address from the address translation buffer TLB and the physical address from the tag memory BAA, the CPU ignores the data read from the units in the buffer storages BSA and BSB, and proceeds with its access to the main storage")*

Claim 6. A semiconductor integrated circuit according to claim 3, comprising:

- a register for holding the logical page address previously inputted to said address conversion memory circuit; *(Column 10, lines 31-37 – State the following: "This arrangement allows a desired logic gate circuit, and hence a desired logic circuit, to be constructed. As a result, the gate array section GA is illustratively used to construct registers, selector circuits and various arithmetic circuits, the registers holding input and output data of the RAM macrocells")*
- a first comparator for comparing a logical page address of the logical address outputted from the memory access circuit with a value of said register; and *(Column 31, lines 56-64 – State the following: "The comparator COM compares the physical address from the address*

translation buffer TLB with the physical address that is output as the tag from the "hit" unit of the tag memory BAA. In case of a match between these addresses, the comparator COM supplies the row selector circuit ROW with a row selection signal for designating the "hit" unit. At this point, the CPU recognizes the hit in the buffer storage and halts its access to the main storage accordingly")

- a second comparator for comparing and judging whether the intra-page address as the remaining lower bits of the relevant logical address is included or not within the boundary area of the address range indicated by the logical page address, *(Column 34, lines 12-21 – Claim ECL differential circuits which act as the proposed second comparator)*
- wherein said switching circuit sets said circuit portion to non-active state when the logical page address is proved to be identical to the preceding logical address based on the result of comparison by said first and second comparators and the intra-page address is not included within said boundary area. *(Column 31, lines 65-68 and Column 32, lines 1-12 – State the following: "In the meantime, read operations on the buffer storages BSA and BSB continue by use of predetermined bits in the logical addresses, in parallel with the compare operation. Stored data is read from the corresponding addresses in a plurality of units, the data being subjected to sequence control provided by the corresponding aligners ALA-ALD. The output signals of these aligners undergo row selection provided by the row selector circuit ROW and are then placed onto the internal bus of the CPU via an output buffer register OBR. Needless to say, if there is no "hit" between the physical address from the address translation buffer TLB and the physical address from the tag memory BAA, the CPU ignores the data read from the units in the buffer storages BSA and BSB, and proceeds with its access to the main storage")*

Claim 7. A semiconductor integrated circuit provided with an address conversion

memory circuit for converting logical address into physical address, comprising: *(Column 31, lines 46-49 – State that there is an address translation buffer that converts the logical address into a physical address)*

- a switching circuit which switches to the active or non-active state *(Column 34, lines 37-47 – State that there is a switching circuit that selectively makes connections)*
- a circuit portion including at least a tag memory for storing a logical page address as the upper bits of the logical address and *(Column 31, lines 49-55 – State the following: "The tag memory BAA performs read operations on a plurality of units by association using predetermined bits of the logical addresses as the search data. In case of a "hit," the corresponding tag i.e., the physical address of the data stored in the buffer storage BSA or BSB, is input to the other input terminal of the comparator COM)*
- a data memory for storing a physical page address as the upper bits of the physical address of said address conversion memory circuit, *(Column 31, lines 65-68 and Column 1, lines 1-12 – State the following: "In the meantime, read operations on the buffer storages BSA and BSB continue by use of predetermined bits in the logical addresses, in parallel with the compare operation. Stored data is read from the corresponding addresses in a plurality of units, the data being subjected to sequence control provided by the corresponding aligners ALA-ALD. The output signals of these aligners undergo row selection provided by the row selector circuit ROW and are then placed onto the internal bus of the CPU via an output buffer register OBR. Needless to say, if there is no "hit" between the physical address from the address translation buffer TLB and the physical address from the tag memory BAA, the CPU ignores the data read from the units in*

the buffer storages BSA and BSB, and proceeds with its access to the main storage)

- wherein supply of clock to said address conversion memory circuit is suspended under the control of said switching circuit during the period where said circuit portion of said address conversion memory circuit is not used and the memory access is executed using the logical address outputted from the circuit of memory access. *(Column 33, lines 26-34 – State the following: "In connection with the arrangement (1) through (7) above, the memory device with logic function has a diagnostic latch circuit which receives the output signals of the sequence control circuits according to a predetermined clock signal and scans the signals out via suitable external terminals. This arrangement enhances the ability of the memory device with logic function comprising a plurality of RAM macrocells to be diagnosed with more ease and efficiency")*

Claim 8. A semiconductor integrated circuit, comprising a processor

- which includes a plurality of sets of a decode circuit to decode instruction codes and an execution circuit to execute said instruction codes, and executes the decode process and execution process of each instruction code of a compressed instruction in the group and arrangement according to instruction location information upon receiving said compressed instruction combining the group information of instruction codes executed simultaneously and the instruction location information indicating arrangement information to suggest a set of decode circuit and execution circuit used to process each instruction code among a plurality of sets thereof, said semiconductor integrated circuit comprising: *(Claim 1, lines 37-61 – State the following: "first decoder means formed along said first direction in an area between said first memory means and said gate array, said first decoder means receiving said address signals from*

said gate array and selecting at least one of said first memory cells; second decoder means formed along said first direction in an area arranged between said second memory means and said gate array, said second decoder means receiving said address signals from said gate array and selecting at least on of said second memory cells; output data selecting means formed in an area arranged between said first memory means and said second memory means and receiving at least one of said first data read out from said first memory cells by said first decoder means, at least one of said second data read out from said second memory cells by said second decoder means and said selection signals from said gate array, said output data selecting means outputting output data out of at least one of said first data and at least one of said second data in predetermined bits and in predetermined combinations to said gate array")

- an expanding circuit for setting to the designated arrangement the instruction codes of the same group which are processed simultaneously according to said instruction location information; *(Column 31, lines 13-21 – Claim sequence control circuits which perform the same functions as the proposed expanding circuit)*
- a detecting circuit for detecting the relevant arrangement based on said instruction location information when the arrangement where a small amount of instruction codes are used and effective instruction codes are not set is generated in a group of instruction codes which are processed simultaneously; *(Column 34, lines 12-21 – Declare parity-check circuits (a.k.a. detection circuits))*
- and a control circuit for setting the execution circuit corresponding to the arrangement where the effective instruction codes are not set to the non-active state based on the detection result of said detecting circuit during the execution period of the relevant group; *(Column 35, lines*

67-68 and Column 36, lines 1-6 – State that there is a write pulse generation circuit which acts like the proposed control circuit)

- wherein said process in the expanding circuit and the detection process by said detecting circuit to the group to be set with said process in the expanding circuit are performed in the same processing cycle. *(Columns 32-34 – Denote that all of the following writings are to be done in a processing cycle)*

Claim 9. A semiconductor integrated circuit according to claim 8,

- wherein said control circuit sets, to the non-active state, the decode circuit corresponding to the arrangement where the effective instruction codes are not set during the decode period of the relevant group based on the detection result of said detecting circuit. *(Claim 1, lines 37-61 – State the following: "first decoder means formed along said first direction in an area between said first memory means and said gate array, said first decoder means receiving said address signals from said gate array and selecting at least one of said first memory cells; second decoder means formed along said first direction in an area arranged between said second memory means and said gate array, said second decoder means receiving said address signals from said gate array and selecting at least on of said second memory cells; output data selecting means formed in an area arranged between said first memory means and said second memory means and receiving at least one of said first data read out from said first memory cells by said first decoder means, at least one of said second data read out from said second memory cells by said second decoder means and said selection signals from said gate array, said output data selecting means outputting output data out of at least one of said first data and at least one of said second data in predetermined bits and in predetermined combinations to said gate array")*

Claim 10. A semiconductor integrated circuit according to claim 8,

- wherein said expanding circuit comprises a buffer memory having a plurality of areas to store a plurality of instruction codes corresponding respectively to a plurality of sets of said decode circuit and execution circuit so that the instruction codes of the same group may be stored to the areas of said buffer memory corresponding to the designated arrangement based on said instruction location information. *(Column 31, lines 56-68 – State that there s buffer storage with areas to store instructions)*

Claim 11. A semiconductor integrated circuit according to claim 9,

- wherein said expanding circuit comprises a buffer memory having a plurality of areas to store a plurality of instruction codes corresponding respectively to a plurality of sets of said decode circuit and execution circuit so that the instruction codes of the same group may be stored to the areas of said buffer memory corresponding to the designated arrangement based on said instruction location information. *(Column 31, lines 56-68 – State that there s buffer storage with areas to store instructions)*

Claim 12. A semiconductor integrated circuit according to claim 11, wherein said processor can process very long instruction words of longer code length. *(Column 30, lines 27-59 – State that there is a processor that is not limited to processing instructions of a certain size)*

Claim 13. A semiconductor integrated circuit according to claim 12, wherein said compressed instruction is the instruction in which said instruction location information is added in place of eliminating the non-executable instruction codes without any effective processes inserted when the number of instruction codes to be executed simultaneously is rather small. *(Column 34, lines 12-21 – State the following: "The RAM macrocells, equipped with read amplifiers which are made up of ECL differential circuits and which simultaneously output multiple bits of stored data at the MOS level, has parity check circuits which receive the output signals of the read*

amplifiers and which are constituted by ECL differential circuits. This arrangement implements RAM macrocells and a memory device with logic function incorporating parity check circuits without the constraint of an appreciably increased delay time in data transmission")

Claim 14. A semiconductor integrated circuit comprising a processor which is provided with a plurality of sets of the decode circuit for decoding instruction codes and the execution circuit for executing said instruction codes and performs the decode process and execution process of each instruction code depending on the instruction in which the instruction codes of the same group to be processed simultaneously are summarized to one instruction code, said semiconductor integrated circuit comprising:
(Claim 1, lines 37-61 – State the following: "first decoder means formed along said first direction in an area between said first memory means and said gate array, said first decoder means receiving said address signals from said gate array and selecting at least one of said first memory cells; second decoder means formed along said first direction in an area arranged between said second memory means and said gate array, said second decoder means receiving said address signals from said gate array and selecting at least on of said second memory cells; output data selecting means formed in an area arranged between said first memory means and said second memory means and receiving at least one of said first data read out from said first memory cells by said first decoder means, at least one of said second data read out from said second memory cells by said second decoder means and said selection signals from said gate array, said output data selecting means outputting output data out of at least one of said first data and at least one of said second data in predetermined bits and in predetermined combinations to said gate array")

- a detecting circuit which reads said instruction into the buffer memory in the processing stage before said decode process and detects whether

the non-executable instruction codes without any effective process is included or not in the relevant instruction; *(Column 34, lines 12-21 – Declare parity-check circuits (a.k.a. detection circuits))*

- and a control circuit which sets the execution circuit of the set to which said non-executable instruction code is sent to non-active state based on the result of said detecting circuit during the execution period of the instruction codes of the same group. *(Column 35, lines 67-68 and Column 36, lines 1-6 – State that there is a write pulse generation circuit which acts like the proposed control circuit)*

Conclusion

3. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lev I. Iwashko whose telephone number is (571)272-1658. The examiner can normally be reached on M-F (alternating Fridays), from 8-4PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim can be reached on (571)272-4182. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lev Iwashko

MATTHEW D. ANDERSON
PRIMARY EXAMINER